19-1313; Rev 0; 11/97

EVALUATION KIT AVAILABLE

MAXIM

High-Speed Step-Down Controller with Synchronous Rectification for CPU Power

General Description

The MAX1638 is an ultra-high-performance, step-down DC-DC controller for CPU power in high-end computer systems. Designed for demanding applications in which output voltage precision and good transient response are critical for proper operation, it delivers over 35A from 1.3V to 3.5V with ±1% total accuracy from a +5V ±10% supply. Excellent dynamic response corrects output transients caused by the latest dynamically clocked CPUs. This controller achieves over 90% efficiency by using synchronous rectification. Flying-capacitor bootstrap circuitry drives inexpensive, external N-channel MOSFETs.

The switching frequency is pin-selectable for 300kHz, 600kHz, or 1MHz. High switching frequencies allow the use of a small surface-mount inductor and decrease output filter capacitor requirements, reducing board area and system cost.

The MAX1638 is available in 24-pin SSOP and QSOP (future package) packages, and offers additional features such as a digitally programmable output; adjustable transient response; and selectable 0.5%, 1%, or 2% AC load regulation. Fast recovery from load transients is ensured by a GlitchCatcher™ current-boost circuit that eliminates delays caused by the buck inductor. Output overvoltage protection is enforced by a crowbar circuit that turns on the low-side MOSFET with 100% duty factor when the output is 200mV above the normal regulation point. Other features include internal digital soft-start, a power-good output, and a 3.5V ±1% reference output.

Applications

Pentium Pro™, Pentium II™, PowerPC™, Alpha™, and K6™ Systems

Workstations

Desktop Computers

LAN Servers

GTL Bus Termination

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1638EAG	-40°C to +85°C	24 SSOP
MAX1638EEG*	-40°C to +85°C	24 QSOP

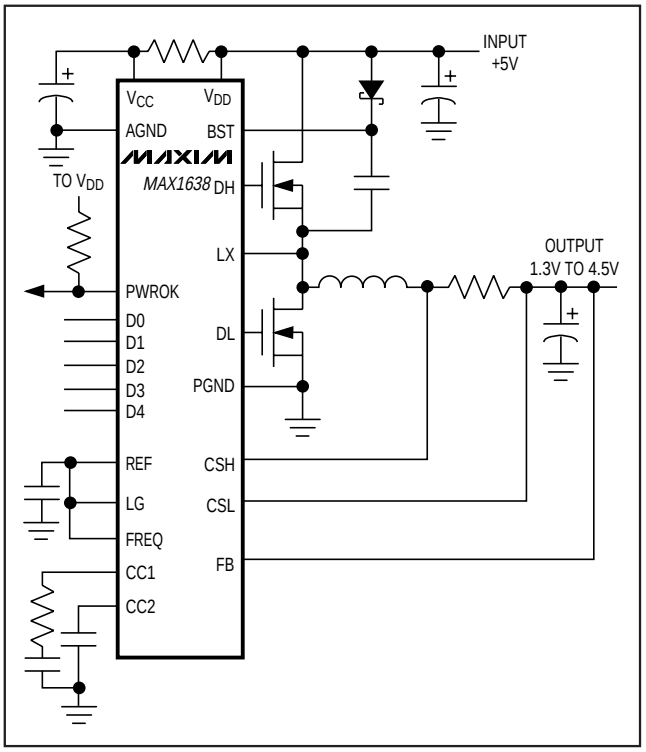
Pin Configuration appears at end of data sheet.
**Future product—contact factory for package availability.*

Pentium Pro and Pentium II are trademarks of Intel Corp.
PowerPC is a trademark of IBM Corp.
Alpha is a trademark of Digital Equipment Corp.
K6 is a trademark of Advanced Micro Devices.
GlitchCatcher is a trademark of Maxim Integrated Products.

Features

- ♦ **Better than ±1% Output Accuracy Over Line and Load**
- ♦ **Greater than 90% Efficiency Using N-Channel MOSFETs**
- ♦ **Pin-Selected High Switching Frequency (300kHz, 600kHz, or 1MHz)**
- ♦ **Over 35A Output Current**
- ♦ **Digitally Programmable Output from 1.3V to 3.5V**
- ♦ **Current-Mode Control for Fast Transient Response and Cycle-by-Cycle Current-Limit Protection**
- ♦ **Short-Circuit Protection with Foldback Current Limiting**
- ♦ **Glitch-Catcher Circuit for Fast Load-Transient Response**
- ♦ **Crowbar Overvoltage Protection**
- ♦ **Power-Good (PWROK) Output**
- ♦ **Digital Soft-Start**
- ♦ **High-Current (2A) Drive Outputs**
- ♦ **Complies with Intel VRM 8.2 Specification**

Typical Operating Circuit



High-Speed Step-Down Controller with Synchronous Rectification for CPU Power

ABSOLUTE MAXIMUM RATINGS

V_{DD}, V_{CC}, PWROK to AGND .....-0.3V to 6V
PGND to AGND .....±0.3V
CSH, CSL to AGND.....-0.3V to (V_{CC} + 0.3V)
NDRV, PDRV, DL to PGND.....-0.3V to (V_{DD} + 0.3V)
REF, CC1, CC2, LG, D0–D4, FREQ,
FB to AGND.....-0.3V to (V_{CC} + 0.3V)
BST to PGND .....-0.3V to 12V
BST to LX .....-0.3V to 6V
DH to LX.....(LX - 0.3V) to (BST + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
QSOP (derate 8.70mW/°C above +70°C).....696mW
QSOP θ_{JC}.....40°C/W
SSOP (derate 8.00mW/°C above +70°C) 640mW
SSOP θ_{JC} .....45°C/W
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range.....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{CC} = D4 = +5V, PGND = AGND = D0–D3 = 0V, FREQ = REF, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Output Voltage (FB) Accuracy	Over line and load (Note 1)		T_A = +25°C to +85°C			±1	%
			T_A = 0°C to +85°C			±1.5	
Input Voltage Range	V_{CC} = V_{DD}			4.5		5.5	V
Input Undervoltage Lockout	V_{CC} rising edge, 1% hysteresis			4.0		4.2	V
V_{CC} Supply Current	V_{CC} = V_{DD} = 5.5V	Operating mode	FB overdrive = 200mV			2.5	mA
			FB overdrive = 0V		5		
		Shutdown mode	DAC code = 11111			0.3	
			V_{REF} = 0V		3.6	10	
V_{DD} Supply Current	V_{CC} = V_{DD} = 5.5V, FB forced 200mV above regulation point, operating or standby mode					0.1	mA
Reference Voltage	No load			3.465	3.5	3.535	V
Reference Load Regulation	0µA < I_{REF} < 100µA					10	mV
Reference Undervoltage Lockout	Rising edge, 1% hysteresis			2.7		3.0	V
Reference Short-Circuit Current	V_{REF} = 0V			0.5		4.0	mA
AC Load Regulation (Note 2)	CSH - CSL = 0mV to 80mV		LG = GND		0.5		%
			LG = REF		1		
			LG = V_{CC}		2		
DC Load Regulation (Note 2)	CSH - CSL = 0mV to 80mV		LG = GND		0.05		%
			LG = REF		0.1		
			LG = V_{CC}		0.2		
PWROK Trip Level	Rising FB, 1% hysteresis with respect to V_{REF}			-7.5	-6	-4.5	%
	Falling FB, 1% hysteresis with respect to V_{REF}			6.5	8	9.5	
PWROK Output Voltage Low	I_{SINK} = 2mA, V_{CC} = 4.5V					0.4	V
PWROK Output Current High	PWROK = 5.5V					1	µA
Switching Frequency	FREQ = V_{CC}			850	1000	1150	kHz
	FREQ = REF			540	600	660	
	FREQ = AGND			255	300	345	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = V_{CC} = D4 = +5V, PGND = AGND = D0–D3 = 0V, FREQ = REF, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Duty Cycle	FREQ = V_{CC}		85	90		%
LG, FREQ Input Voltage	GND (low)				0.2	V
	REF (mid)		3.3		3.7	
	V_{CC} (high)		V_{CC} - 0.1			
Logic Input Voltage Low	D0–D4, V_{CC} = 4.5V				0.8	V
Logic Input Voltage High	D0–D4, V_{CC} = 5.5V		2.0			V
D0–D4 Source Current	D0–D4 = 0V		2	5	10	µA
LG, FREQ Input Current					4	µA
CSH, CSL Input Current	CSH = CSL = 1.3V, D0–D3 = 5V, D4 = 0V				50	µA
FB Input Current					±0.1	µA
CC1 Output Resistance				10		kΩ
CC2 Transconductance				1		mmho
CC2 Clamp Voltage	Minimum		2.4		3.0	V
	Maximum		4		V_{CC}	
CC2 Source/Sink Current	100mV overdrive			100		µA
DH On-Resistance	BST - LX = 4.5V			0.7	2	Ω
DL On-Resistance	V_{DD} = 4.5V			0.7	2	Ω
DH, DL Source/Sink Current	DH = DL = 2.5V			2		A
DH, DL Dead Time			0	30		ns
PDRV Trip Level	With respect to V_{REF}, FB going low	T_A = +25°C	-2.75	-2	-1.25	%
		T_A = 0°C to +85°C	-3		-1	
NDRV Trip Level	With respect to V_{REF}, FB going high	T_A = +25°C	1.25	2	2.75	%
		T_A = 0°C to +85°C	1		3	
PDRV, NDRV Response Time	FB overdrive = 5%			75		ns
PDRV, NDRV On-Resistance	V_{DD} = 4.5V			2	5	Ω
PDRV, NDRV Source/Sink Current	PDRV = NDRV = 2.5V			0.5		A
PDRV, NDRV Minimum On-Time				100		ns
Current-Limit Trip Voltage	FB = 3.5V		85	100	115	mV
	FB = 0V (Foldback)		15	38	70	
Soft-Start Time	To full current limit			1536		1 / f_{OSC}
BST Leakage Current	BST = 12V, LX = 7V, REF = GND				50	µA

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{CC} = D4 = +5V, PGND = AGND = D0–D3= 0V, FREQ = REF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Input Voltage Range	V_{CC} = V_{DD}			4.5		5.5	V
Input Undervoltage Lockout	V_{CC} rising edge, 1% hysteresis			3.9		4.3	V
V_{CC} Supply Current	V_{CC} = V_{DD} = 5.5V, FB overdrive = 200mV	Operating mode				3	mA
		Shutdown mode	DAC code = 11111			0.4	
			V_{REF} = 0V			12	
V_{DD} Supply Current	V_{CC} = V_{DD} = 5.5V, FB forced 200mV above regulation point, operating or shutdown mode					0.2	mA
Reference Voltage	No load			3.448	3.5	3.553	V
Output Voltage (FB) Accuracy	Over line and load (Note 1)					±2.5	%
PWROK Trip Level	Rising FB, 1% hysteresis with respect to V_{REF}			-8	-6	-4	%
	Falling FB, 1% hysteresis with respect to V_{REF}			6	8	10	
Switching Frequency	FREQ = V_{CC}			800	1000	1200	kHz
	FREQ = REF			510	600	690	
	FREQ = AGND			240	300	360	
Maximum Duty Cycle	FREQ = V_{CC}			84	90		%
DH On-Resistance	BST - LX = 4.5V				0.7	2	Ω
DL On-Resistance	V_{DD} = 4.5V				0.7	2	Ω
Current-Limit Trip Voltage	FB = 3.5V			70	100	130	mV

Note 1: FB accuracy is 100% tested at FB = 3.5V (code 10000) with V_{CC} = V_{DD} = 4.5V to 5.5V and CSH - CSL = 0mV to 80mV. The other DAC codes are tested with V_{CC} = V_{DD} = 5V and CSH - CSL = 0.

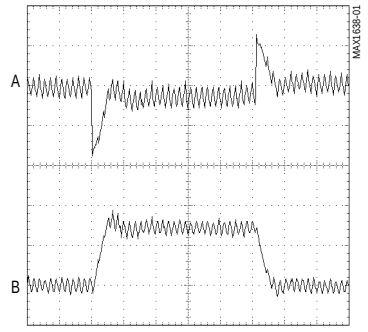
Note 2: AC load regulation sets the AC loop gain, to make tradeoffs between output filter capacitor size and transient response, and has only a slight effect on DC accuracy or DC load-regulation error.

Note 3: Specifications from 0°C to -40°C are guaranteed by design, not production tested.

Typical Operating Characteristics

(T_A = +25°C, using the MAX1638 evaluation kit, unless otherwise noted.)

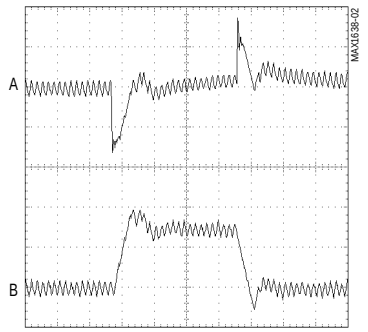
LOAD-TRANSIENT RESPONSE WITHOUT GLITCHCATCHER (C_{OUT} = 880µF)



10µs/div

V_{IN} = 5V, V_{OUT} = 2.0V, LOAD = 14A, 3A/µs
A: V_{OUT}, 50mV/div, AC COUPLED
B: INDUCTOR CURRENT, 10A/div

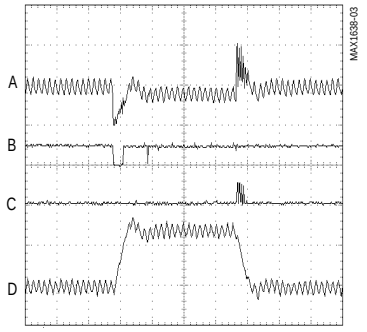
LOAD-TRANSIENT RESPONSE WITHOUT GLITCHCATCHER (C_{OUT} = 440µF)



10µs/div

V_{IN} = 5V, V_{OUT} = 2.0V, LOAD = 14A, 3A/µs
A: V_{OUT}, 100mV/div, AC COUPLED
B: INDUCTOR CURRENT, 10A/div

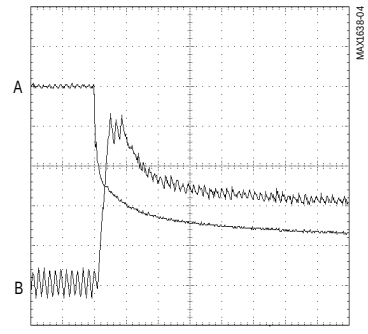
LOAD-TRANSIENT RESPONSE WITH GLITCHCATCHER



10µs/div

C_{OUT} = 440µF, V_{IN} = 5V, V_{OUT} = 2.0V, LOAD = 14A, 30A/µs
A: V_{OUT}, 100mV/div, AC COUPLED
B: PDRV, 5V/div
C: NDRV, 5V/div
D: INDUCTOR CURRENT, 10A/div

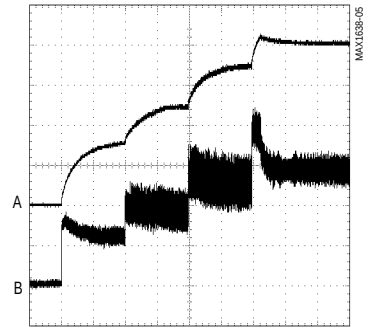
FOLDBACK CURRENT LIMIT



10µs/div

V_O = 2.0V NOMINAL
A: V_{OUT} = 0.5V/div
B: INDUCTOR CURRENT, 5A/div

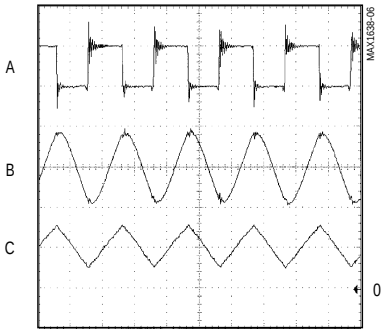
START-UP WAVEFORMS



400µs/div

A: V_{OUT} = 0.5V/div
B: INDUCTOR CURRENT, 5A/div

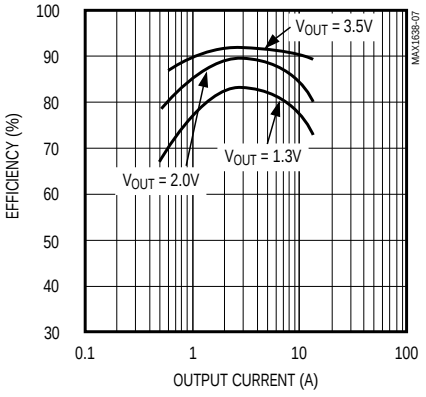
SWITCHING WAVEFORMS



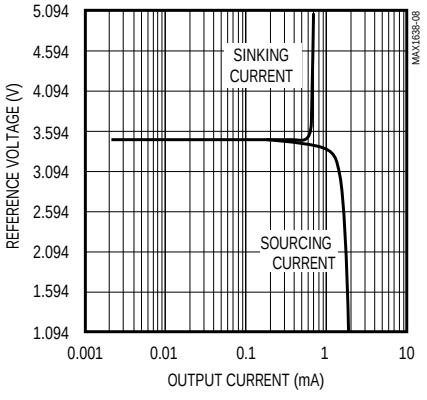
1µs/div

V_{IN} = 5V, V_{OUT} = 2.5V, LOAD = 5A
A: LX, 5V/div
B: V_{OUT}, 20mV/div, AC COUPLED
C: INDUCTOR CURRENT, 5A/div

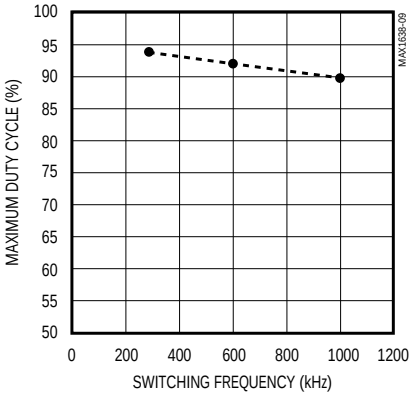
EFFICIENCY vs. OUTPUT CURRENT



REFERENCE VOLTAGE vs. OUTPUT CURRENT



MAXIMUM DUTY CYCLE vs. SWITCHING FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1	BST	Boost-Capacitor Bypass for High-Side MOSFET Gate Drive. Connect a 0.1µF capacitor and low-leakage Schottky diode as a bootstrapped charge-pump circuit to derive a 5V gate drive from V_{DD} for DH.
2	PWROK	Open-Drain Logic Output. PWROK is high when the voltage on FB is within +8% and -6% of its set-point.
3	CSL	Current-Sense Amplifier's Inverting Input. Place the current-sense resistor very close to the controller IC, and use a Kelvin connection.
4	CSH	Current-Sense Amplifier's Noninverting Input
5, 6, 7	D2, D1, D0	Digital Inputs for Programming the Output Voltage. D0–D4 are logic inputs that set the output to a voltage between 1.3V and 3.5V (Table 2). D0–D4 are internally pulled up to V_{CC} with 5µA current sources.
8	LG	Loop Gain-Control Input. LG is a three-level input that is used to trade off loop gain vs. AC load-regulation and load-transient response. Connect LG to V_{CC}, REF, or AGND for 2%, 1%, or 0.5% AC load-regulation errors, respectively.
9	V_{CC}	Analog Supply Input, 5V. Use an RC filter network, as shown in Figure 1.
10	REF	Reference Output, 3.5V. Bypass REF to AGND with 0.1µF (min). Sources up to 100µA for external loads. Force REF below 2V to turn off the controller.
11	AGND	Analog Ground
12	FB	Voltage-Feedback Input. Connect FB to the CPU's remote voltage-sense point. The voltage at this input is regulated to a value determined by D0–D4.
13	CC1	Fast-Loop Compensation Capacitor Input. Connect a ceramic capacitor and resistor in series from CC1 to AGND. See the section *Compensating the Feedback Loop*.
14	CC2	Slow-Loop Compensation Capacitor Input. Connect a ceramic capacitor from CC2 to AGND. See the section *Compensating the Feedback Loop*.
15	FREQ	Frequency-Select Input. FREQ = V_{CC}: 1MHz FREQ = REF: 600kHz FREQ = AGND: 300kHz
16, 17	D4, D3	Digital Inputs for Programming the Output Voltage
18	NDRV	GlitchCatcher N-Channel MOSFET Driver Output. NDRV swings between V_{DD} and PGND.
19	PDRV	GlitchCatcher P-Channel MOSFET Driver Output. PDRV swings between V_{DD} and PGND.
20	V_{DD}	5V Power Input for MOSFET Drivers. Bypass V_{DD} to PGND within 0.2 in. (5mm) of the V_{DD} pin using a 0.1µF capacitor and 4.7µF capacitor connected in parallel.
21	DL	Low-Side Synchronous Rectifier Gate-Drive Output. DL swings between PGND and V_{DD}. See the section *BST High-Side Gate-Driver Supply and MOSFET Drivers*.
22	PGND	Power Ground
23	LX	Switching Node. Connect LX to the high-side MOSFET source and inductor.
24	DH	High-Side Main MOSFET Switch Gate-Drive Output. DH is a floating driver output that swings from LX to BST, riding on the LX switching-node voltage. See the section *BST High-Side Gate-Driver Supply and MOSFET Drivers*.

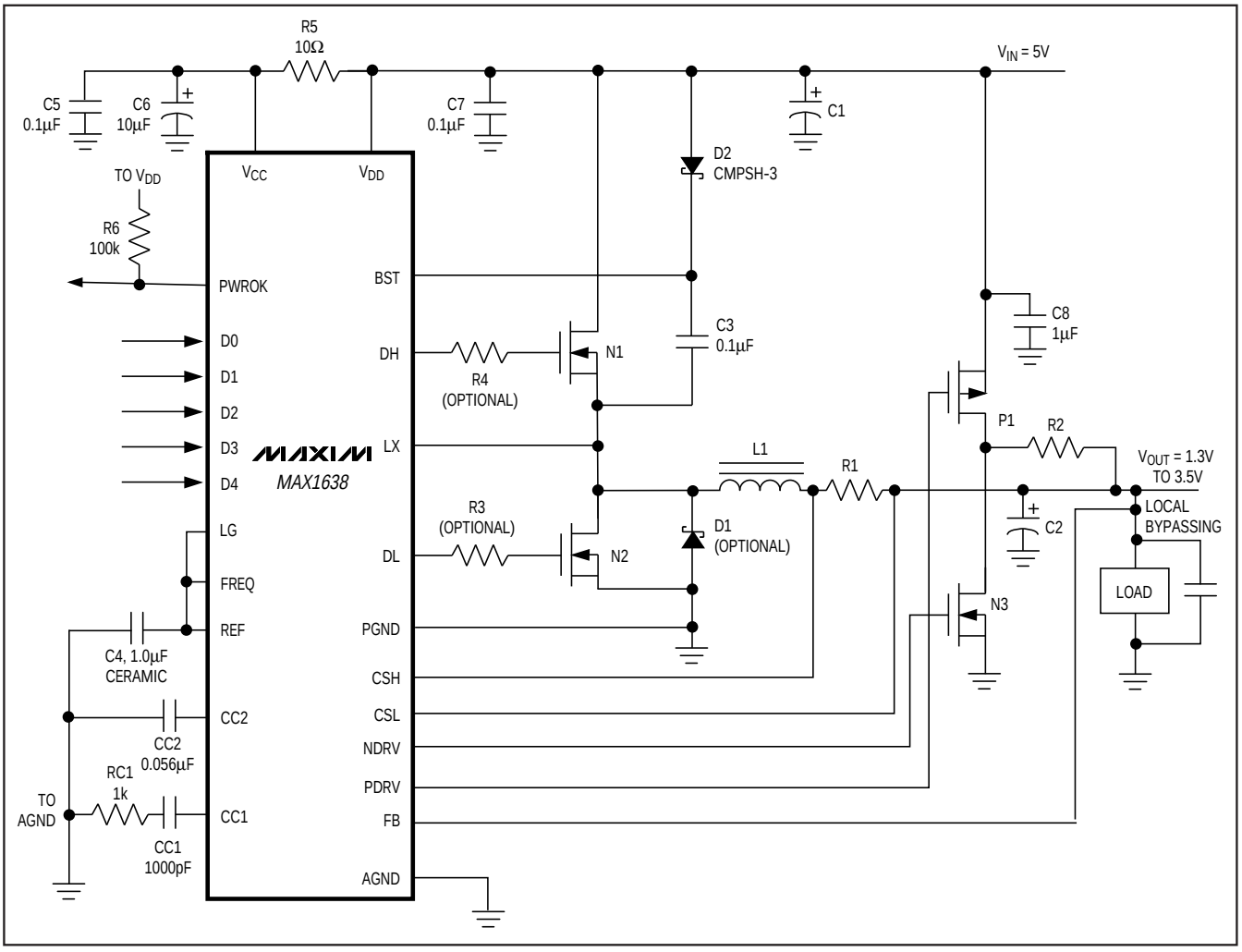


Figure 1. Standard Application Circuit

Standard Application Circuits

The predesigned MAX1638 circuit shown in Figure 1 meets a wide range of applications with output currents up to 19A and higher. Use Table 1 to select components appropriate for the desired output current range, and adapt the evaluation kit PC board layout as necessary. This circuit represent a good set of trade-offs between cost, size, and efficiency while staying within the worst-case specification limits for stress-related parameters, such as capacitor ripple current.

The MAX1638 circuit was designed for the specified frequency. Do not change the switching frequency without first recalculating component values—particularly the inductance, output filter capacitance, and RC1 resistance values. Table 2 lists the voltage adjustment DAC codes.

Detailed Description

The MAX1638 is a BiCMOS power-supply controller designed for use in switch-mode, step-down (buck) topology DC-DC converters. Synchronous rectification provides high efficiency. It is intended to provide the high precision, low noise, excellent transient response, and high efficiency required in today's most demanding applications.

High-Speed Step-Down Controller with Synchronous Rectification for CPU Power

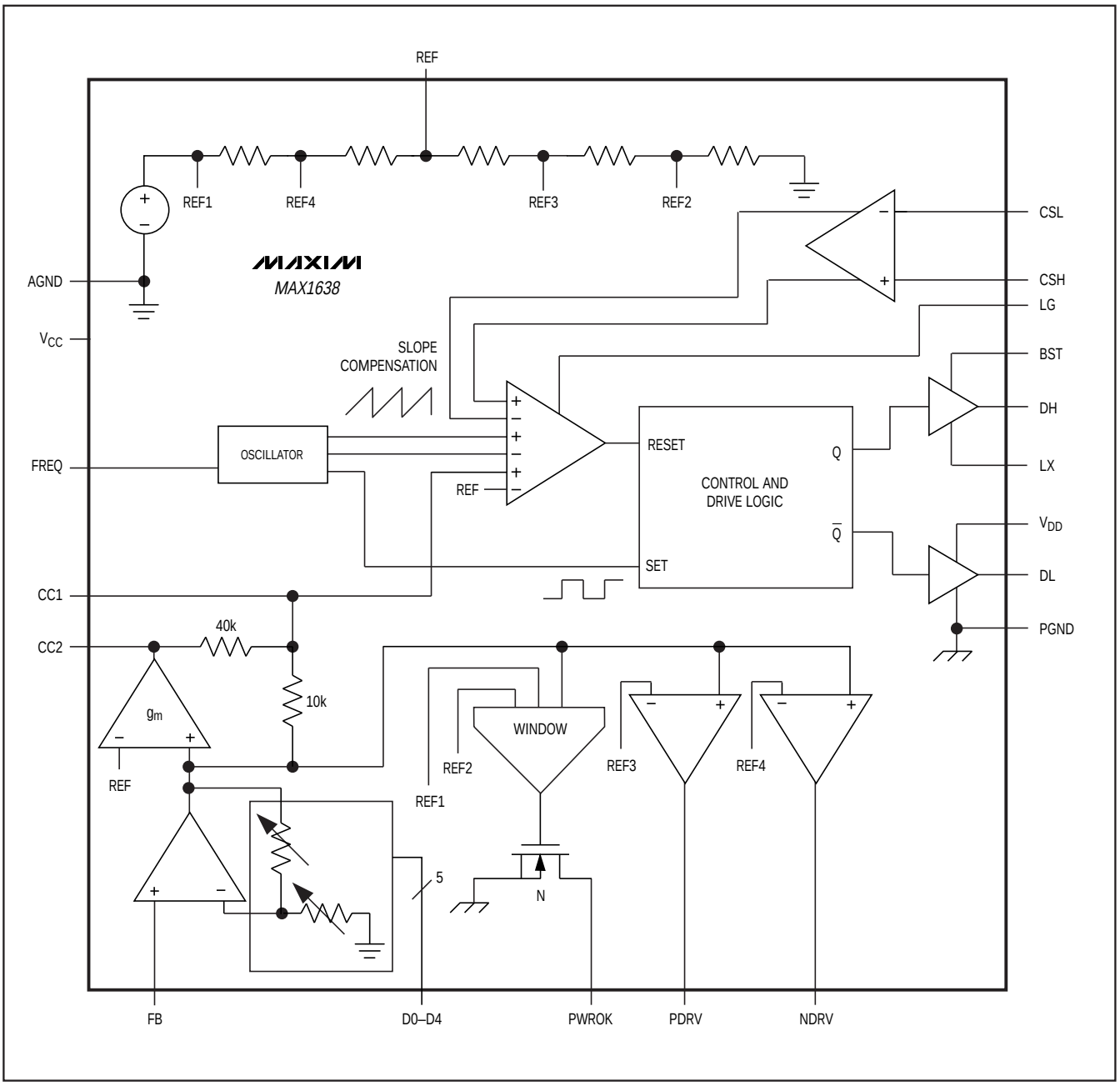


Figure 2. Simplified Block Diagram

Table 1. Component List for Standard Applications

COMPONENT	LOAD REQUIREMENT		
	2.0V, 14A	**2.0V, 19A**	**1.3V, 19A**
C1	**(x3) Sanyo OS-CON 10SA220M (220µF)**	(x4) Sanyo/OS-CON 10SA220M (220µF)	(x4) Sanyo/OS-CON 10SA220M (220µF)
C2	**(x4) Sanyo OS-CON 4SP220M (220µF)**	(x6) Sanyo OS-CON 4SP220M (220µF)	(x7) Sanyo OS-CON 4SP220M (220µF)
D1 (optional)	Nihon NSQ03A02 Schottky diode or Motorola MBRS340	Nihon NSQ03A02 Schottky diode or Motorola MBRS340	Nihon NSQ03A02 Schottky diode or Motorola MBRS340
D2	**Central Semiconductor CMPSH-3**	Central Semiconductor CMPSH-3	Central Semiconductor CMPSH-3
L1	**Coiltronics UP4-R47 (0.47µH, 19A, SMD)** or Panasonic ETQP1F0R7H (0.70µH, 19A, 1.6mΩ, SMD)	Panasonic ETQP2F1R0S (0.70µH, 23A, 0.94mΩ, SMD)	Panasonic ETQP2F1R0S (0.70µH, 23A, 0.94mΩ, SMD)
N1	**Fairchild FDB7030L (10mΩ)** or Int'l Rectifier IRL3803S (9mΩ)	(x2) Fairchild FDB7030L (10mΩ) or (x2) Int'l Rectifier IRL3803S (9mΩ)	(x2) Fairchild FDB7030L (10mΩ) or (x2) Int'l Rectifier IRL3803S (9mΩ)
N2	**Fairchild FDB7030L (10mΩ)** or Int'l Rectifier IRL3803S (9mΩ)	(x2) Fairchild FDB7030L (10mΩ) or (x2) Int'l Rectifier IRL3803S (9mΩ)	(x2) Fairchild FDB7030L (10mΩ) or (x2) Int'l Rectifier IRL3803S (9mΩ)
P1/N3 (optional)	Int'l Rectifier IRF7105 (0.4Ω/0.16Ω)	Int'l Rectifier IRF7307 (0.09Ω/0.05Ω)	Int'l Rectifier IRF7307 (0.09Ω/0.05Ω)
R1	**(x2) Dale WSL-2512-R009-F (10mΩ)**	(x2) Dale WSR-20.007 ±1% (7mΩ)	(x2) Dale WSR-20.007 ±1% (7mΩ)
R2 (optional)	Dale WSL-2512-R120-J (120mΩ)	—	—

Note: *Parts used in evaluation board are shown in bold.*

PWM Controller Block and Integrator

The heart of the current-mode PWM controller is a multi-input open-loop comparator that sums three signals (Figure 2): the buffered feedback signal, the current-sense signal, and the slope-compensation ramp. This direct-summing configuration approaches ideal cycle-by-cycle control over the output voltage. The output voltage error signal is generated by an error amplifier that compares the amplified feedback voltage to an internal reference.

Each pulse from the oscillator sets the main PWM latch that turns on the high-side switch for a period determined by the duty factor (approximately V_{OUT} / V_{IN}). The current-mode feedback system regulates the peak inductor current as a function of the output voltage error signal. Since average inductor current is nearly the same as peak current (assuming the inductor value is set relatively high to minimize ripple current), the circuit acts as a switch-mode transconductance amplifier. It pushes the second output LC filter pole, normally found in a duty-factor-controlled (voltage-mode) PWM, to a higher frequency. To preserve inner-loop stability and eliminate regenerative inductor current staircasing, a slope-compensation ramp is summed into the main PWM comparator. Under fault conditions where the inductor current exceeds the maximum current-limit threshold, the high-side latch resets, and the high-side switch turns off.

Internal Reference

The internal 3.5V reference (REF) is accurate to ±1% from 0°C to +85°C, making REF useful as a system reference. Bypass REF to AGND with a 0.1µF (min) ceramic capacitor. A larger value (such as 2.2µF) is recommended for high-current applications. Load regulation is 10mV for loads up to 100µA. Reference undervoltage lockout is between 2.7V and 3V. Short-circuit current is less than 4mA.

Synchronous-Rectifier Driver

Synchronous rectification reduces conduction losses in the rectifier by shunting the normal Schottky diode or MOSFET body diode with a low-on-resistance MOSFET switch. The synchronous rectifier also ensures proper start-up by precharging the boost-charge pump used for the high-side switch gate-drive circuit. Thus, if you must omit the synchronous power MOSFET for cost or other reasons, replace it with a small-signal MOSFET, such as a 2N7002.

The DL drive waveform is simply the complement of the DH high-side drive waveform (with typical controlled dead time of 30ns to prevent cross-conduction or shoot-through). The DL output's on-resistance is 0.7Ω (typ) and 2Ω (max).

BST High-Side Gate-Driver Supply and MOSFET Drivers

Gate-drive voltage for the high-side N-channel switch is generated using a flying-capacitor boost circuit (Figure 3). The capacitor is alternately charged from the +5V supply and placed in parallel with the high-side MOSFET's gate and source terminals.

Gate-drive resistors (R3 and R4) can often be useful to reduce jitter in the switching waveforms by slowing down the fast-slewing LX node and reducing ground bounce at the controller IC. However, switching loss may increase. Low-value resistors from around 1Ω to 5Ω are sufficient for many applications.

GlitchCatcher Current-Boost Driver

Drivers for an optional GlitchCatcher current-boost circuit are included in the MAX1638 to improve transient response in applications where several amperes of load current are required in a matter of a few tens of nanoseconds. The GlitchCatcher can be used to offset the fast drop in output voltage due to the ESR of the output capacitance. The current-boost circuit improves transient response by providing a direct path from the input to the output that circumvents the buck inductor's filtering action. When the output drops out of regulation by more than 2%, the P-channel or N-channel switch turns on and injects current directly into the output from V_{IN} or ground, forcing the output back into regulation. The driver's response time is typically 75ns, and minimum on-time is typically 100ns. GlitchCatcher provides the greatest benefit when the output voltage is less than 2V, and in applications using minimum output capacitance.

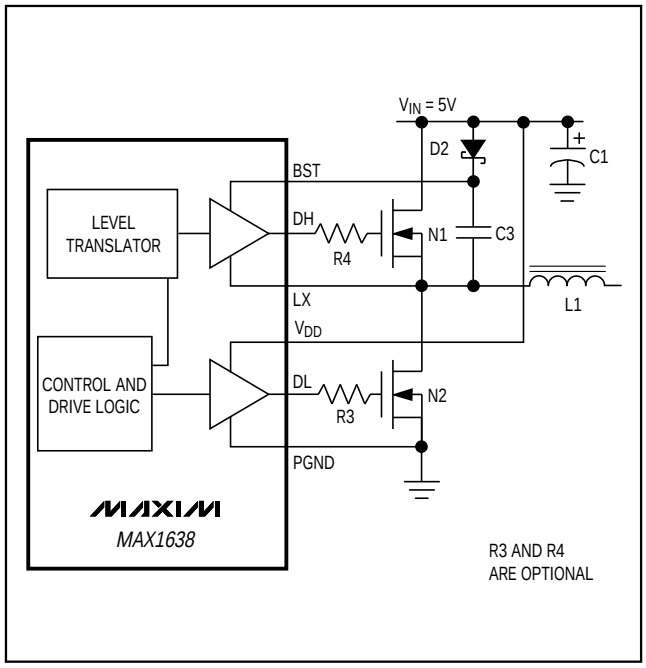


Figure 3. Boost Supply for Gate Drivers

Current Sense and Overload Current Limiting

The current-sense circuit resets the main PWM latch and turns off the high-side MOSFET switch whenever the voltage difference between CSH and CSL from current through the sense resistor (R1) exceeds the peak current limit (100mV typical).

Current-mode control provides cycle-by-cycle current-limit capability for maximum overload protection. During normal operation, the peak current limit set by the current-sense resistor determines the maximum output current. When the output is shorted, the peak current may be higher than the set current limit due to delays in the current-sense comparator. Thus, foldback current limiting is employed where the set current-limit point is reduced from 100mV to 38mV as the output (feedback) voltage falls (Figure 4). When the short-circuit condition is removed, the feedback voltage will rise and the current-limit voltage will revert to 100mV. The foldback current-limit circuit is designed to ensure startup into a resistive load.

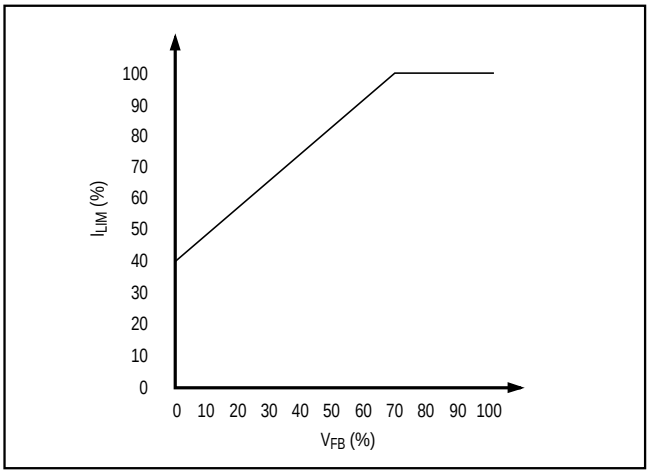


Figure 4. Foldback Current Limit

High-Side Current Sensing

The common-mode input range of the current-sense inputs (CSH and CSL) extends to V_{CC}, so it is possible to configure the circuit with the current-sense resistor on the input side rather than on the load side (Figure 5). This configuration improves efficiency by reducing the power dissipation in the sense resistor according to the duty ratio.

In the high-side configuration, if the output is shorted directly to GND through a low-resistance path, the current-sense comparator may be unable to enforce a current limit. Under such conditions, circuit parasitics such as MOSFET $R_{DS(ON)}$ typically limit the short-circuit current to a value around the peak-current-limit setting.

Attach a lowpass-filter network between the current-sense pins and resistor to reduce high-frequency common-mode noise. The filter should be designed with a time constant of around one-fifth of the on-time (130ns at 600kHz, for example). Resistors in the 20Ω to 100Ω range are recommended for R7 and R8. Connect the filter capacitors C11 and C12 from V_{CC} to CSH and CSL, respectively.

Values of 39Ω and 3.3nF are suitable for many designs. Place the current-sense filter network close to the IC, within 0.1 in (2.5mm) of the CSH and CSL pins.

Overvoltage Protection

When the output exceeds the set voltage, the synchronous rectifier (N2) is driven high (and N1 is driven low). This causes the inductor to quickly dissipate any stored energy and force the fault current to flow to ground. Current is limited by the source impedance and parasitic resistance of the current path, so a fuse is required in series with the +5V input to protect against low-impedance faults, such as a shorted high-side MOSFET. Otherwise, the low-side MOSFET will eventually fail. DL will go low if the input voltage drops below the undervoltage lockout point.

Internal Soft-Start

Soft-start allows a gradual increase of the internal current limit at start-up to reduce input surge currents. An internal DAC raises the current-limit threshold from 0V to 100mV in four steps (25mV, 50mV, 75mV, and 100mV) over the span of 1536 oscillator cycles.

Design Procedure

Setting the Output Voltage

Select the output voltage using the D0–D4 pins. The MAX1638 uses an internal 5-bit DAC as a feedback-resistor voltage divider. The output voltage can be digitally set from 1.3V to 3.5V using the D0–D4 inputs (Table 2).

D0–D4 are logic inputs and accept both TTL and CMOS voltage levels. The MAX1638 has both FB and AGND inputs, allowing a Kelvin connection for remote voltage and ground sensing to eliminate the effects of trace resistance on the feedback voltage. (See *PC Board Layout Considerations* for further details.) FB input current is 0.1µA (max).

The MAX1638 DAC codes (D0–D4) were designed for compatibility with the Intel VRM 8.2 specification for output voltages between 1.8V (code 00101) and 3.5V (code 10000). Codes 00110 to 01111 have also been designed for 50mV increments, allowing set voltages down to 1.300V. Code 11111 turns off the buck controller, placing the IC in a shutdown mode (0.2mA typical).

Choosing the Error-Amplifier Gain

Set the error-amplifier gain to match the voltage-precision requirements of the CPU used. The MAX1638's loop-gain control input (LG) allows trade-offs in DC/AC voltage accuracy versus output filter capacitor requirements. AC load regulation can be set to 0.5%, 1%, or 2% by connecting LG as shown in Table 3.

DC load regulation is typically 10 times better than AC load regulation, and is determined by the gain set by the LG pin.

High-Speed Step-Down Controller with Synchronous Rectification for CPU Power

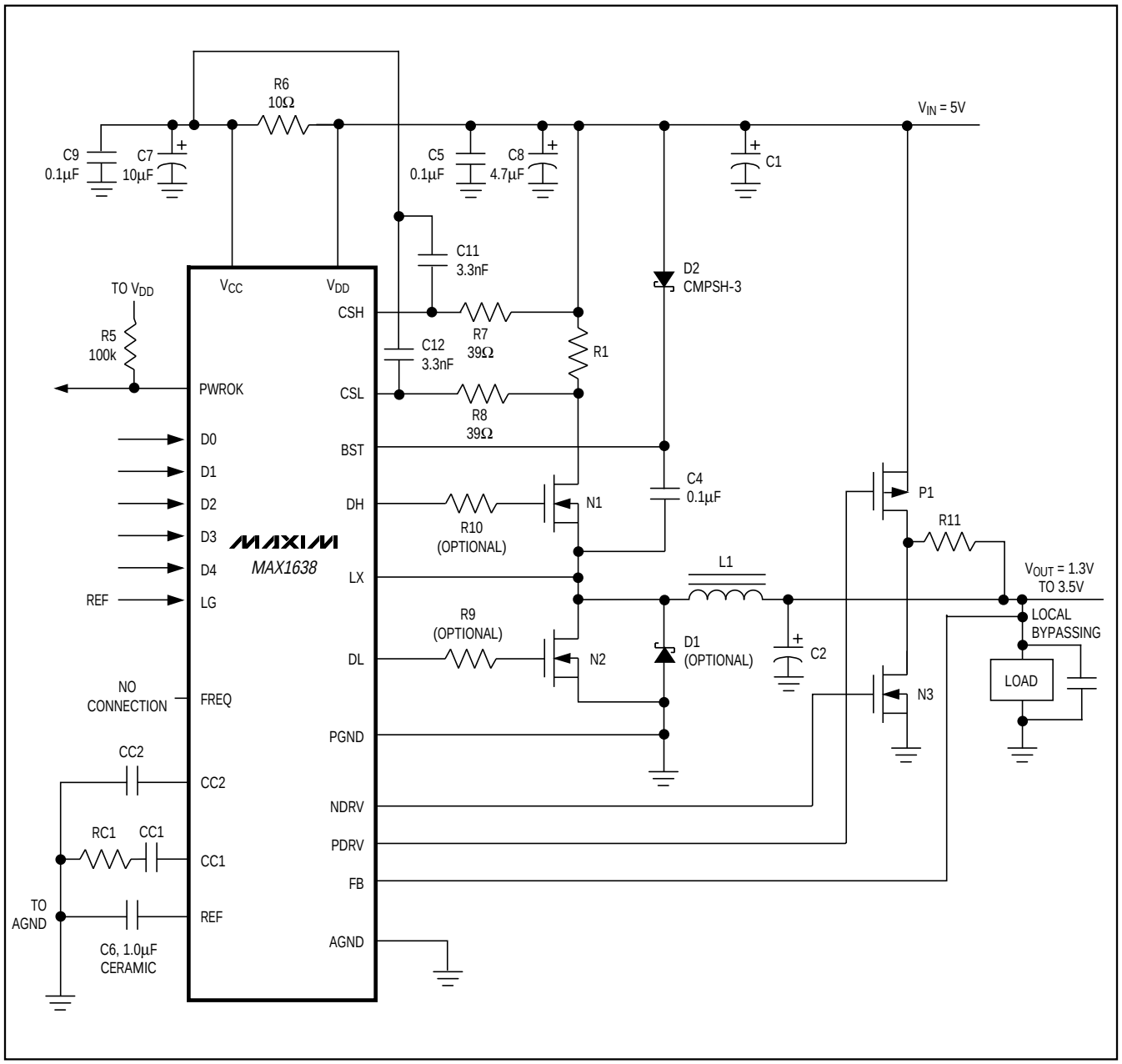


Figure 5. Buck Regulator with High-Side Current Sensing

Table 2. Output Voltage Adjustment Settings

D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)	COMPATIBILITY
0	0	0	0	0	2.050	Intel-compatible DAC codes
0	0	0	0	1	2.000	
0	0	0	1	0	1.950	
0	0	0	1	1	1.900	
0	0	1	0	0	1.850	
0	0	1	0	1	1.800	
0	0	1	1	0	1.750	Continuation of 50mV increment to 1.3V
0	0	1	1	1	1.700	
0	1	0	0	0	1.650	
0	1	0	0	1	1.600	
0	1	0	1	0	1.550	
0	1	0	1	1	1.500	
0	1	1	0	0	1.450	
0	1	1	0	1	1.400	
0	1	1	1	0	1.350	
0	1	1	1	1	1.300	
1	0	0	0	0	3.500	Intel-compatible DAC codes
1	0	0	0	1	3.400	
1	0	0	1	0	3.300	
1	0	0	1	1	3.200	
1	0	1	0	0	3.100	
1	0	1	0	1	3.000	
1	0	1	1	0	2.900	
1	0	1	1	1	2.800	
1	1	0	0	0	2.700	
1	1	0	0	1	2.600	
1	1	0	1	0	2.500	
1	1	0	1	1	2.400	
1	1	1	0	0	2.300	
1	1	1	0	1	2.200	
1	1	1	1	0	2.100	
1	1	1	1	1	N/A	Shutdown

Specifying the Inductor

Three key inductor parameters must be specified: inductance value (L), peak current (I_{PEAK}), and DC resistance (R_{DC}). The following equation includes a constant LIR, which is the ratio of inductor peak-to-peak AC current to DC load current. Typically LIR can be between 0.1 to 0.5. A higher LIR value allows for smaller inductors and better transient response, but results in higher losses and output ripple. A good compromise between size and loss is a 30% ripple current to load current ratio (LIR = 0.30), which corresponds to a peak inductor current 1.15 times higher than the DC load current.

Table 3. LG Pin Adjustment Settings

LG CONNECTED TO:	AC LOAD-REGULATION ERROR (%)	DC LOAD-REGULATION ERROR (%)	TYPICAL A_E (V_{GAIN}/ I_{GAIN})
V_{CC}	2	0.2	2
REF	1	0.1	4
GND	0.5	0.05	8

$$L = \frac{V_{OUT}\left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times f_{OSC} \times I_{OUT} \times LIR}$$

where f is the switching frequency, between 300kHz and 1MHz; I_{OUT} is the maximum DC load current; and LIR is the ratio of AC to DC inductor current (typically 0.3). The exact inductor value is not critical and can be adjusted to make trade-offs among size, transient response, cost, and efficiency. Although lower inductor values minimize size and cost, they also reduce efficiency due to higher peak currents. In general, higher inductor values increase efficiency, but at some point resistive losses due to extra turns of wire exceed the benefit gained from lower AC current levels. Load-transient response can be adversely affected by high inductor values, especially at low (V_{IN} - V_{OUT}) differentials.

The peak inductor current at full load is 1.15 x I_{OUT} if the previous equation is used; otherwise, the peak current can be calculated using the following equation:

$$I_{PEAK} = I_{OUT} + \frac{V_{OUT}\left(V_{IN(MAX)} - V_{OUT}\right)}{2f_{OSC} \times L \times V_{IN(MAX)}}$$

The inductor's DC resistance is a key parameter for efficient performance, and should be less than the current-sense resistor value.

Calculating the Current-Sense Resistor Value

Calculate the current-sense resistor value according to the worst-case minimum current-limit threshold voltage (from the *Electrical Characteristics*) and the peak inductor current required to service the maximum load.

Use I_{PEAK} from the equation in the section *Specifying the Inductor*.

$$R_{SENSE} = \frac{85mV}{I_{PEAK}}$$

The high inductance of standard wire-wound resistors can degrade performance. Low-inductance resistors, such as surface-mount power metal-strip resistors, are preferred. The current-sense resistor's power rating should be higher than the following:

$$P_{SENSE} \geq \frac{(115mV)^2}{R_{SENSE}}$$

In high-current applications, connect several resistors in parallel as necessary to obtain the desired resistance and power rating.

Selecting the Output Filter Capacitor

Output filter capacitor values are generally determined by effective series resistance (ESR) and voltage-rating requirements, rather than by the actual capacitance value required for loop stability. Due to the high switching currents and demanding regulation requirements in a typical MAX1638 application, use only specialized low-ESR capacitors intended for switching-regulator applications, such as Kemet T510, AVX TPS, Sprague 595D, Sanyo OS-CON, or Sanyo GX series. Do not use standard aluminum-electrolytic capacitors, which can cause high output ripple and instability due to high ESR. The output voltage ripple is usually dominated by the filter capacitor's ESR, and can be approximated as $I_{RIPPLE} \times R_{ESR}$. To ensure stability, the capacitor must meet *both* minimum capacitance and maximum ESR values as given in the following equations:

$$C_{OUT} > \frac{V_{REF}\left(1 + \frac{V_{OUT}}{V_{IN(MIN)}}\right)}{V_{OUT} \times R_{SENSE} \times f_{OSC}}$$

$$R_{ESR} < R_{SENSE}$$

Compensating the Feedback Loop

The feedback loop needs proper compensation to prevent excessive output ripple and poor efficiency caused by instability. Compensation cancels unwanted poles and zeros in the DC-DC converter's transfer function that are due to the power-switching and filter elements with corresponding zeros and poles in the feedback network. These compensation zeros and poles are set by the compensation components CC1, CC2, and RC1. The objective of compensation is to ensure stability by ensuring that the DC-DC converter's phase shift is less than 180° by a safe margin, at the frequency where the loop gain falls below unity.

Canceling the Sampling Pole and Output Filter ESR Zero

Compensate the fast-voltage feedback loop by connecting a resistor and a capacitor in series from the CC1 pin to AGND. The pole from CC1 can be set to cancel the zero from the filter-capacitor ESR. Thus the capacitor at CC1 should be as follows:

$$CC1 = \frac{C_{OUT} \times R_{ESR}}{10k\Omega}$$

Resistor RC1 sets a zero that can be used to compensate for the sampling pole generated by the switching frequency. Set RC1 to the following:

$$RC1 = \frac{\left(1 + \frac{V_{OUT}}{V_{IN}}\right)}{2f_{OSC} \times CC1}$$

The CC1 pin's output resistance is 10kΩ.

Setting the Dominant Pole and Canceling the Load and Output Filter Pole

Compensate the slow-voltage feedback loop by adding a ceramic capacitor from the CC2 pin to AGND. This is an integrator loop used to cancel out the DC load-regulation error. Selection of capacitor CC2 sets the dominant pole and a compensation zero. The zero is typically used to cancel the unwanted pole generated by the load and output filter capacitor at the maximum load current. Select CC2 to place the zero close to or slightly lower than the frequency of the unwanted pole, as follows:

$$CC2 = \frac{1mmho \times C_{OUT}}{4} \times \frac{V_{OUT}}{I_{OUT(MAX)}}$$

The transconductance of the integrator amplifier at CC2 is 1mmho. The voltage swing at CC2 is internally clamped around 2.4V to 3V minimum and 4V to V_{CC} maximum to improve transient response times. CC2 can source and sink up to 100µA.

Choosing the MOSFET Switches

The two high-current N-channel MOSFETs must be logic-level types with guaranteed on-resistance specifications at V_{GS} = 4.5V. Lower gate-threshold specs are better (i.e., 2V max rather than 3V max). Gate charge

should be less than 200nC to minimize switching losses and reduce power dissipation.

I^2R losses are the greatest heat contributor to MOSFET power dissipation and are distributed between the high- and low-side MOSFETs according to duty factor, as follows:

$$P_D \text{ (high side)} = I_{LOAD}^2 \times R_{DS(ON)} \times \frac{V_{OUT}}{V_{IN}}$$

$$P_D \text{ (low side)} = I_{LOAD}^2 \times R_{DS(ON)} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Gate-charge losses are dissipated in the IC, and do not heat the MOSFETs. Ensure that both MOSFETs are at a safe junction temperature by calculating the temperature rise according to package thermal-resistance specifications. The high-side MOSFET's worst-case dissipation occurs at the maximum output voltage and minimum input voltage. For the low-side MOSFET, the worst case is at the maximum input voltage when the output is short-circuited (consider the duty factor to be 100%).

Calculating IC Power Dissipation

Power dissipation in the IC is dominated by average gate-charge current into both MOSFETs. Average current is approximately:

$$I_{DD} = (Q_{G1} + Q_{G2}) \times f_{OSC}$$

where I_{DD} is the drive current, Q_G is the total gate charge for each MOSFET, and f_{OSC} is the switching frequency.

Power dissipation of the IC is:

$$P_D = I_{CC} \times V_{CC} + I_{DD} \times V_{DD}$$

where I_{CC} is the quiescent supply current of the IC.

Junction temperature for the IC is primarily a function of the PC board layout, since most of the heat is removed through the traces connected to the pins and the ground and power planes. A 24-pin SSOP on a typical four-layer board with ground and power planes show equivalent thermal impedance of about 60°C/W. Junction temperature of the die is approximately:

$$T_J = P_D \times \theta_{JA} + T_A$$

where T_A is the ambient temperature and θ_{JA} is the equivalent junction-to-ambient thermal impedance.

Selecting the Rectifier Diode

The rectifier diode D1 is a clamp that catches the negative inductor swing during the 30ns typical dead time between turning off the high-side MOSFET and turning on the low-side MOSFET synchronous rectifier. D1 must be a Schottky diode, to prevent the MOSFET body diode from conducting. It is acceptable to omit D1 and let the body diode clamp the negative inductor swing, but efficiency will drop about 1%. Use a 1N5819 diode for loads up to 3A, or a 1N5822 for loads up to 10A.

Adding the BST Supply Diode and Capacitor

A signal diode, such as a 1N4148, works well for D2 in most applications, although a low-leakage Schottky diode provides slightly improved efficiency. Do not use large power diodes, such as the 1N4001 or 1N5817. Exercise caution in the selection of Schottky diodes, since some types exhibit high reverse leakage at high operating temperatures. Bypass BST to LX using a 0.1µF capacitor.

Selecting the Input Capacitors

Place a 0.1µF ceramic capacitor and 10µF capacitor between V_{CC} and AGND, as well as between V_{DD} and PGND, within 0.2 in. (5mm) of the V_{CC} and V_{DD} pins.

Select low-ESR input filter capacitors with a ripple-current rating exceeding the RMS input ripple current, connecting several capacitors in parallel if necessary. RMS input ripple current is determined by the input voltage and load current, with the worst-possible case occurring at $V_{IN} = 2 \times V_{OUT}$:

$$I_{RMS} = I_{LOAD\ (MAX)} \frac{\sqrt{V_{OUT}\ (V_{IN} - V_{OUT})}}{V_{IN}}$$

$$I_{RMS} = I_{OUT} / 2 \text{ when } V_{IN} = 2V_{OUT}$$

Choosing the GlitchCatcher MOSFETs

P-channel and N-channel switches and a series resistor are required for the current-boost circuit (Figure 6). Current through the MOSFETs and current-limiting resistors must be sufficient to supply the load current, with enough extra for prompt output regulation without excessive overshoot. Design for boost-current values 1.5 times the maximum load current, and choose MOSFETs and current-limiting resistors such that:

$$R_{DSON,P(MAX)} + R_{LIMIT} \approx \frac{V_{IN} - V_{OUT}}{1.5\ I_{OUT(MAX)}}$$

and

$$R_{DSON,N(MAX)} + R_{LIMIT} \approx \frac{V_{OUT}}{1.5\ I_{OUT(MAX)}}$$

Gate resistors may be required to slow the transition edges.

High-Speed Step-Down Controller with Synchronous Rectification for CPU Power

Applications Information

Efficiency Considerations

Refer to the MAX796–MAX799 data sheet for information on calculating losses and improving efficiency.

PC Board Layout Considerations

Good PC board layout and routing are *required* in high-current, high-frequency switching power supplies to achieve good regulation, high efficiency, and stability. The PC board layout artist must be provided with explicit instructions concerning the placement of power-switching components and high-current routing. It is strongly recommended that the evaluation kit PC board layouts be followed as closely as possible. Contact Maxim's Applications Department concerning the availability of PC board examples for higher-current circuits.

In most applications, the circuit is on a multilayer board, and full use of the four or more copper layers is recommended. Use the top layer for high-current power and ground connections. Leave the extra copper on the board as a pseudo-ground plane. Use the bottom layer for quiet connections (REF, FB, AGND), and the inner layers for an uninterrupted ground plane. A ground plane and pseudo-ground plane are essential for reducing ground bounce and switching noise.

Place the high-power components (C1, R1, N1, D1, N2, L1, and C2 in Figure 1) as close together as possible.

Minimize ground-trace lengths in high-current paths. The surface-mount power components should be butted up to one another with their ground terminals almost touching. Connect their ground terminals using a wide, filled zone of top-layer copper (the pseudo-ground plane), rather than through the internal ground plane. At the output terminal, use vias to connect the top-layer pseudo-ground plane to the normal inner-layer ground plane at the output filter capacitor ground terminals. This minimizes interference from IR drops and ground noise, and ensures that the IC's AGND is sensing at the supply's output terminals.

Minimize high-current path trace lengths. Use very short and wide traces. From C1 to N1: 0.4 in. (10mm) max length; D1 anode to N2: 0.2 in. (5mm) max length; LX node (N1 source, N2 drain, D1 cathode, inductor L1): 0.6 in. (15mm) max length.

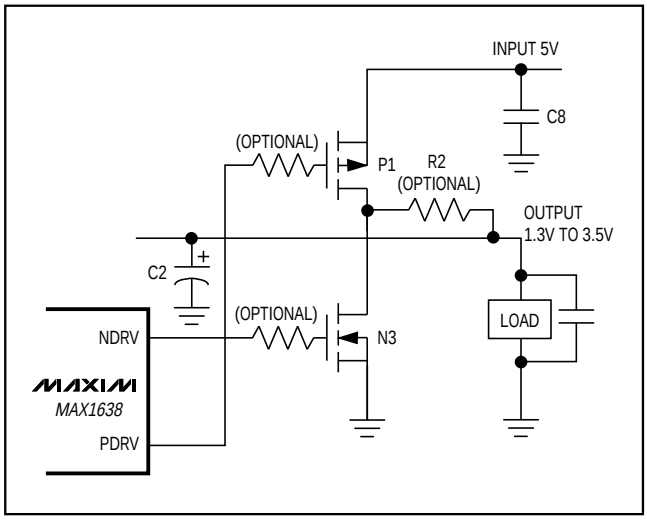
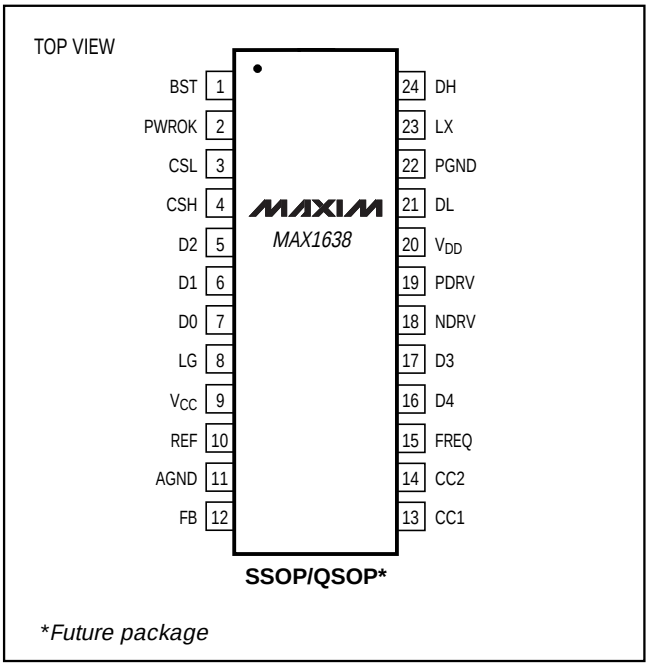


Figure 6. GlitchCatcher Circuit

Pin Configuration



**Future package*

Chip Information

TRANSISTOR COUNT: 3135

SUBSTRATE CONNECTED TO AGND